

[c6] 6. The structure of claim 1, wherein the drain region and the first conductive type second well region are short-circuited.

[c7] 7. The structure of claim 1, wherein the drain region and the first conductive type second well region are short-circuited by a second contact penetrating through a junction between the drain region and the first conductive type second well region.

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[c8] 8. The structure of claim 1, wherein the structure further comprises:
an interlayer dielectric layer disposed on the first conductive type substrate;
a plug disposed in the interlayer dielectric layer and electrically connected with the second contact; and
a conductive line disposed on the interlayer dielectric layer and electrically connected with the plug.

[c9] 9. The structure of claim 1, wherein the dopants of the doped region, the source region and the drain region are the same.

[c10] 10. A fabrication method for a flash memory device, comprising:
providing a first conductive type substrate, wherein the substrate comprises a second conductive type first well region, a first conductive type second well region and a stacked gate structure which are sequentially formed thereon;
forming a source region and a drain region in the substrate beside two sides of the stacked gate structure;
forming a spacer on a sidewall of the stacked gate structure;
forming a first patterned photoresist layer on the substrate, the first patterned photoresist layer exposes the substrate at the drain region;
etching the substrate at the drain region until penetrating through the junction between the drain region and the first conductive type second well region by using the first patterned photoresist layer and the stacked gate structure with the spacer as a mask;
removing the first patterned photoresist layer;
forming a second patterned photoresist layer on the substrate, the second patterned photoresist layer exposes the substrate at the source region;
etching the substrate at the source region to the second conductive type first